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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,372	02/01/2001	Jiann-Cheng Chen	0325.00446	8121

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CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

EXAMINER

SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 03/19/2004

3

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/775,372

Applicant(s)

CHEN ET AL.

Examiner

Suresh K Suryawanshi

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 February 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4 and 7-17 is/are rejected.
- 7) ☒ Claim(s) 3,5,6 and 18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 February 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: _____

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DETAILED ACTION

1. Claims 1-18 are presented for examination.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Information Disclosure Statement

3. The information disclosure statement filed 4/11/01 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered (Other Documents).

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Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slate (US Patent no 4,392,021) in view of Furumochi et al (US Patent no 5,986,967).

6. As per claims 1, 16 and 17, Slate teaches

a first logic circuit comprising one or more counters [fig. 7; col. 9, line 63 – col. 10, line 11]; and

a second logic circuit configured to detect and present a faster clock signal of said synchronized clocked signals [fig. 7; col. 12, lines 48-57; a faster clock detector].

Slate does not expressly disclose about a synchronization circuit. However, a routineer in the art would realize that it is possible to add a synchronization circuit as disclosed by Furumochi et al where a plurality of input clocks can be synced with each other [col. 2, lines 5-8; a synchronization circuit, which receives a plurality of input signals]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as a synchronization circuit will eliminate a wasteful consumption of power by

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the circuit when it is operated in response to a sync signal. Moreover, this will also eliminate the need of a separate sync circuit for each clock and thus reducing the size of the total circuit design.

7. As per claim 2, Slate teaches that first logic circuit comprises digital fast clock detection circuit [fig. 7; col. 12, lines 48-57; a faster clock detector].

8. As per claim 4, Slate discloses the invention substantially. Slate does not disclose expressly that a fast clock detect circuit with programmable resolution configured to control a resolution of said apparatus. However, Slate has disclosed a fast clock detection circuit [fig. 7] and a programmable divide-by-N counter [fig. 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify the Slate's invention with a programmable resolution configuration to control a resolution of said apparatus.

9. As per claim 7, Slate discloses the invention substantially. Slate does not disclose expressly that said apparatus is configured to synchronously select said faster clock signal. However, a routineer in the art would realize that after implementing the synchronization circuit as disclosed by Furumochi et al [col. 2, lines 5-8; a synchronization circuit, which receives a plurality of input signals], apparatus will be configured to synchronously select faster clock signal. Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to modify the Slate's invention with a synchronization circuit as mentioned by Furumochi et al to eliminate a wasteful consumption of power by the circuit when it is

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operated in response to a sync signal. Moreover, this will also eliminate the need of a separate circuit for each clock and thus reducing the size of the total circuit design.

10. As per claims 8 -14, Slate discloses the invention substantially. Slate does not disclose expressly that the apparatus is fully configured. However, a routineer in the art will be able to reconfigure the apparatus upon reading the full discloser. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to reconfigure Slate's apparatus as desired.

11. As per claim 15, Slate discloses the invention substantially. Slate discloses about a faster clock detect circuit [fig. 7; col. 12, lines 48-57; a faster clock detector], but does not disclose having two different circuitry. One for detection and another for selection. However, a routineer in the art will be able to modify Slate's circuitry, as detection and selection circuitries are well known. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Slate's apparatus with a faster detection circuit and a selection circuit.

Slate does not expressly disclose about a synchronization circuit. However, a routineer in the art would realize that it is possible to add a synchronization circuit as disclosed by Furumochi et al where a plurality of input clocks can be synced with each other [col. 2, lines 5-8; a synchronization circuit, which receives a plurality of input signals]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the

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cited references as a synchronization circuit will eliminate a wasteful consumption of power by the circuit when it is operated in response to a sync signal. Moreover, this will also eliminate the need of a separate circuit for each clock and thus reducing the size of the total circuit design.

Claim Objections

12. Claims 3, 5, 6 and 18 are objected to because of the following informalities: dependent claims of rejected independent claims.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

sks

March 17, 2004


THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100